WHAT IS CLAIMED IS:

1. A memory device comprising:

a nonvolatile first data area that stores first data that are not encrypted and that can be read and written;

a nonvolatile first key data area that stores first key data that can be written but can not be read;

a nonvolatile second key data area that stores second key data that can be written but can not be read; and

a controller that allows reading or writing of the first data when the first key data matches with the second key data.

2. The memory device according to claim 1, further comprising a comparing unit that compares the first key data with the second key data, wherein

the controller allows the reading or the writing of the first data based on the result of comparison performed by the comparing unit.

3. The memory device according to claim 2, if the first key data match second key data, the comparing unit authorizes the reading or the writing of the first data, and if the first key data do not match the second key data, the comparing unit inhibits the reading and the writing of the first data.

4. The memory device according to claim 1, further comprising a nonvolatile second data area that stores second data that can be read

and written, and that are obtained by encrypting the first key data.

5. The memory device according to claim 4, further comprising a comparing unit that compares the first key data with the second key data, wherein

the controller allows the reading or the writing of the second data based on the result of comparison performed by the comparing unit.

6. The memory device according to claim 5, wherein if the first key data match the second key data, the comparing unit authorizes the reading or the writing of the second data, and if the first key data do not match the second key data, the comparing unit authorizes only the reading but inhibits the writing of the second data.

7. The memory device according to claim 1, further comprising a third data area that stores third data that are set when the first key data are stored, and are cleared when the first key data is reset.

8. The memory device according to claim 1, further comprising a communication unit that receives the first data, the first key data, and the second key data from outside, and output the first data to the outside.

9. The memory device according to claim 1, wherein the memory

device is driven by an external electric power supply.

10. The memory device according to claim 1, wherein the first data area is divided into a plurality of sub data areas each containing the first data, the first key data area is divided into a plurality of sub key data areas each containing the first key data, the second key data area is divided into a plurality of sub key registers each containing the second key data, and if the first key data stored in a desired one of the sub first key data areas matches with the second key data stored in a corresponding one of the sub second key data areas, the controller allows the reading or the writing of the first data in a corresponding of the sub data area.

11. The memory device according to claim 10, wherein all the sub data areas have same memory capacity.

12. The memory device according to claim 10, wherein each of the sub data area has a different memory capacity.

13. The memory device according to claim 10, wherein a memory capacity of each of the sub data area is set based on a length of data to be stored in the sub data area.

14. The memory device according to claim 1, wherein the first data area and the first key data area are composed of a ferroelectric memory

that holds the data by means of remnant polarization.

15. A memory access limiting system, comprising:

a memory device that includes

a nonvolatile first data area that stores first data that are not encrypted and that can be read and written;

a nonvolatile first key data area that stores first key data that can be written but can not be read;

a nonvolatile second key data area that stores second key data that can be written but can not be read; and

a controller that allows reading or writing of the first data when the first key data matches with the second key data;

a writing unit that writes the first data into the first data area and the first key data into the first key data area;

a first interface unit that is used for transmission and reception of data between the writing unit and the memory device;

a reading/writing unit that writes the second key data into the second key data area, and accesses the first data area for reading and writing the first data; and

a second interface unit that is used for transmission and reception of data between the reading/writing unit and the memory device.

16. The memory access limiting system according to claim 15, further comprising a comparing unit that compares the first key data

with the second key data, wherein

the controller allows the reading or the writing of the first data based on the result of comparison performed by the comparing unit.

17. The memory access limiting system according to claim 16, if the first key data match second key data, the comparing unit authorizes the reading or the writing of the first data, and if the first key data do not match the second key data, the comparing unit inhibits the reading and the writing of the first data.

18. The memory access limiting system according to claim 15, further comprising a nonvolatile second data area that stores second data that can be read and written, and that are obtained by encrypting the first key data.

19. The memory access limiting system according to claim 18, further comprising a comparing unit that compares the first key data with the second key data, wherein

the controller allows the reading or the writing of the second data based on the result of comparison performed by the comparing unit.

20. The memory access limiting system according to claim 19, wherein if the first key data match the second key data, the comparing unit authorizes the reading or the writing of the second data, and if the

first key data do not match the second key data, the comparing unit authorizes only the reading but inhibits the writing of the second data.

21. The memory access limiting system according to claim 15, further comprising a third data area that stores third data that are set when the first key data are stored, and are cleared when the first key data is reset.

22. The memory access limiting system according to claim 15, wherein the memory device further includes a communication unit that receives the first data, the first key data, and the second key data from the writing unit via the first interface unit, and outputs the first data to the reading/writing unit via the second interface unit.

23. The memory access limiting system according to claim 15, wherein the memory device is driven by an external electric power supply.

24. The memory access limiting system according to claim 15, wherein the first data area is divided into a plurality of sub data areas each containing the first data, the first key data area is divided into a plurality of sub key data areas each containing the first key data, the second key data area is divided into a plurality of sub key registers each containing the second key data, and if the first key data stored in a desired one of the sub first key data areas matches with the second

key data stored in a corresponding one of the sub second key data areas, the controller allows the reading or the writing of the first data in a corresponding of the sub data area.

25. The memory access limiting system according to claim 24, wherein all the sub data areas have same memory capacity.

26. The memory access limiting system according to claim 24, wherein each of the sub data area has a different memory capacity.

27. The memory access limiting system according to claim 24, wherein a memory capacity of each of the sub data area is set based on a length of data to be stored in the sub data area.

28. The memory access limiting system according to claim 15, wherein the first data area and the first key data area are composed of a ferroelectric memory that holds the data by means of remnant polarization.

29. A memory access method, comprising:

a first writing that includes writing a predetermined unencrypted data into a nonvolatile first data area from which data can be read and written after resetting the first data area, and writing key data into a nonvolatile second data area into which data can be written but can not be read;

inhibiting the reading and the writing of the first data;

a second writing that includes writing temporary key data into a nonvolatile key register, into which data can be written but can not be read when the reading and the writing of the first data are inhibited; and

authorizing the reading or writing of the first data when the temporary key data match the key data, whereas inhibiting the reading and the writing of the first data when the temporary key data do not match the key data.

30. The memory access method according to claim 29, before the second writing, further comprising:

encrypting and writing the key data as encrypted data, into a nonvolatile second data area that stores second data that can be read and written; and

reading and decrypting the encrypted data so as to acquire the key data,

wherein the key data acquired by decrypting the encrypted data are written as the temporary key data into the key register at the second writing.